# WEST Search History

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DATE: Monday, March 21, 2005

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| ☐ | L82 | L72 and L81 | 6 |
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| ☐ | L80 | L48 and L77 | 1 |
| ☐ | L79 | L32 and L77 | 1 |
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| ☐ | L74 | L21 and L72 | 974 |
| ☐ | L73 | L48 and L72 | 19 |
| ☐ | L72 | packet switch$3 | 17799 |
| ☐ | L71 | sun.as. and treat.xp. and L21 | 8 |
| ☐ | L70 | L21 same L69 | 31 |
| ☐ | L69 | instruction block$1 | 1864 |
| ☐ | L68 | L21 and L66 | 5 |
| ☐ | L67 | packet$1 and L66 | 13 |
| ☐ | L66 | decoupled processor$1 | 56 |
| ☐ | L65 | L64 adj processor$1 | 5 |
| ☐ | L64 | non-blocking or nonblocking | 6386 |
| ☐ | L63 | mon-blocking or nonblocking | 1219 |
| ☐ | L62 | L21 with L48 | 17 |
| ☐ | L61 | L21 adj processor | 629 |
| ☐ | L60 | L48 and L53 | 1 |
| ☐ | L59 | L45 and L53 | 3 |
| ☐ | L58 | L53 and L57 | 1 |
| ☐ | L57 | (712/32).ccls. | 355 |
| ☐ | L56 | context switch$3 same L42 | 29 |
| ☐ | L55 | L42 and L53 | 1 |
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| ☐ | L53 | (712/235).ccls. | 171 |
| ☐ | L52 | packet$1.ti,ab,clm. and L51 | 8 |

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| ☐ | L51 | L48 with (parallel or pipelin$3) | 124 |
| ☐ | L50 | packet$1.ti,ab,clm. and L48 | 72 |
| ☐ | L49 | packet.ti,ab,clm. and L48 | 58 |
| ☐ | L48 | subprocessor$1 or sub-processor$1 | 1025 |
| ☐ | L47 | L21 same L45 | 28 |
| ☐ | L46 | packet$1 same L45 | 16 |
| ☐ | L45 | non-blocking with processor$1 | 332 |
| ☐ | L44 | L43 not L41 | 5 |
| ☐ | L43 | L42 and L36 | 14 |
| ☐ | L42 | packet with processor$1 | 11300 |
| ☐ | L41 | L32 and L36 | 9 |
| ☐ | L40 | packet$1 and L35 | 22 |
| ☐ | L39 | L35 and L38 | 7 |
| ☐ | L38 | conditional branch$3 | 5109 |
| ☐ | L37 | L35 and L36 | 0 |
| ☐ | L36 | (712/234).ccls. | 332 |
| ☐ | L35 | serial processors | 97 |
| ☐ | L34 | L21 with L32 | 24 |
| ☐ | L33 | L21 and L32 | 151 |
| ☐ | L32 | packet processor$1 | 1420 |
| ☐ | L31 | L30 not private branch exchange | 33 |
| ☐ | L30 | L28 not L29 | 44 |
| ☐ | L29 | branch$3 same L27 | 5 |
| ☐ | L28 | branch$3 and L27 | 49 |
| ☐ | L27 | L21 same L24 | 221 |
| ☐ | L26 | branch$3 and L25 | 453 |
| ☐ | L25 | L21 and L24 | 2571 |
| ☐ | L24 | decoupled | 26329 |
| ☐ | L23 | L21 and L22 | 4 |
| ☐ | L22 | decoupled architecture | 29 |
| ☐ | L21 | multi-threading or multithreading or thread$1 | 286029 |
| ☐ | L20 | chained processor$1 | 8 |
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| ☐ | L18 | L17 with buffer$1 | 0 |
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| ☐ | L16 | L12 and L15 | 2 |
| ☐ | L15 | 709/$.ccls. | 34918 |

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|---|---|---|---|
| ☐ | L14 | router$1 and L12 | 17 |
| ☐ | L13 | L11 and L12 | 2 |
| ☐ | L12 | reservation station$1 | 995 |
| ☐ | L11 | internet protocol or tcp | 59908 |
| ☐ | L10 | L8 and L9 | 18 |
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| ☐ | L8 | internet protocol or ip or tcp | 113147 |
| ☐ | L7 | reservation station$1 and L6 | 10 |
| ☐ | L6 | (data or network) adj packet$1 | 42938 |
| ☐ | L5 | (router$1 or switch$2) and L4 | 76 |
| ☐ | L4 | packet$1 and reservation station$1 | 143 |
| ☐ | L3 | L1 same next instruction | 18 |
| ☐ | L2 | pipeline stage$1 with conditional branch$3 | 105 |
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END OF SEARCH HISTORY